

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Takahisa YAMAHA

Serial No.: 09/518,709

Filed: March 3, 2000

Our Ref.: P/2171-180

Date: March 12, 2001

Group Art Unit: 2812

Examiner: --



RECEIVED
MAR 20 2001
MAIL ROOM

2812
#4/F
3
Wash. D.C.
3-30-01

For: MANUFACTURE METHOD FOR SEMICONDUCTOR WITH SMALL VARIATION IN MOS THRESHOLD VOLTAGE

Assistant Commissioner of Patents
Washington, D.C. 20231

SUBMISSION

Sir:

<input checked="" type="checkbox"/>	Submitted herewith is a copy of art together with an art listing form listing the same for the convenience of the Examiner.
<input checked="" type="checkbox"/>	The Japanese Publication(s) listed on the attached art listing form was/were cited in a Japanese Office Action issued in a related application. A copy of the Office Action is attached. English-language Abstracts have been provided for the references.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to:
Assistant Commissioner of Patents, Washington, D.C. 20231, on March 12, 2001.

Steven I. Weisburd

Name of applicant, assignee or
Registered Representative

Signature

March 12, 2001
Date of Signature

Respectfully submitted,

Steven I. Weisburd

Registration No.: 27,409

OSTROLENK, FABER, GERB & SOFFEN, LLP

1180 Avenue of the Americas

New York, New York 10036-8403

Telephone: (212) 382-0700

SIW:sks/Enclosures